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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,447	12/23/1999	ROBERT BEDICHEK	TRANS18	7416

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EXAMINER	
MAKHDOOM, SAMARINA	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 12/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/471,447	Applicant(s) BEDICHEK ET AL.
	Examiner Samarina Makhdoom	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawing correction submitted on 11/8/2002 was accepted by the examiner.

Response to Arguments

2. Applicant's arguments filed 11/08/02 have been fully considered but they are not persuasive.

3. Applicant argues in substance that, (1) Nicolas, Goettelmann, and Fogg all fail to disclose determining validity of a translation of a target instruction linked to an earlier translation; (2) de Nicolas, Goettelmann, and Fogg all fail to the memory address of the target instruction is tested against a copy of the memory address of the target instruction from which a translation of the target instruction was made; (3) De Nicolas, Goettelmann, and Fogg all fail to disclose testing a memory address of a target instruction to be executed as a part of a process that is separate from the translation of the target instruction. (4) De Nicolas, Goettelmann, and Fogg all fail to disclose testing the memory address as a part of the translation of the target instruction; (5) De Nicolas, Goettelmann, and Fogg all fail to disclose copying a memory address of a target instruction when a translation of the target instruction is made and linked to an earlier translation.

4. As to points (1) – (5), (1) the examiner respectfully disagrees. As recited in the previous office action De Nicolas teaches on column 5, lines 38-46 the comparison of run time address to the previously loaded address and if the addresses match, then the location of the return is the same. Thus, if the addresses match, then the validity is determined. Therefore, De Nicolas

meets the claimed limitation. Moreover, Goettelmann and Fogg similarly teach the comparisons to determine the validity of a translation. Specifically, see the abstract of Goettelmann and the abstract of Fogg. (2) See the response to argument (1) above. (3) Goettelmann discloses in Figure 4, testing the memory address as a separate procedure, See Col. 8, lines 1-42, for creating an actual machine address space image of the memory addresses to ensure the translation will work from one computer to another. As for De Nicolas, See Col. 6, lines 1-7 where the invention checks or tests any instruction that updates memory to determine if memory is modified. As for Fogg, See Col. 5, line 66 to Col. 6, line 5. (4) Goettelmann discloses testing memory address space as part of a translation, See Figure 8, and text in Col. 13, lines 25-58 where the translated software has all the referenced addresses with in the image. The invention accommodates the differences in two address spaces thereby testing the memory address. As for Fogg, See Figure 9, and text in Col. 15, line 56 to Col. 16, line 34, the translated code is stored in the memory area and the shared memory area checks or tests the addresses to ensure proper simulation of the software. As for De Nicholas, the rejection is withdrawn to Claims 3 and 10. (5) Goettelmann discloses copying a memory address of a target instruction when a translation of the target instruction is made and linked to an earlier translation, See Figure 23, and text in Col. 30 lines 5-57, where the translation of a target instruction such as service calls are linked into a single address area based on the target machine system software. As for Fogg, and De Nicholas, the rejection to claims 4 and 11 is withdrawn.

5. The newly added Claim 15 is rejected in Goettelmann below.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Goettelmann et al. U.S. Patent No. 5,313,614.

As per Claims 1 and 8, Goettelmann et al. recite translating an instruction set from a target computer to the host computer and validating the translation by testing the memory address and executing the translation or generating an exception based on the test. See Col. 9, lines 43-58.

As per Claims 2 and 9, Goettelmann et al. disclose the step of testing a memory address of the translated instruction in a process separate from translating the target instruction. See Col 9, lines 58-62.

As per Claims 3 and 10, Goettelmann et al. disclose the step testing the memory address of a target instruction as part of the translation of the target instruction. See Col. 20, lines 62-66.

As per Claims 4 and 11, Goettelmann et al. disclose the step of copying a memory address of a target instruction and linking it to an earlier translation. See Col. 30, lines 6-12.

As per Claims 5 and 12, Goettelmann et al. disclose the step copying and storing the memory address of the target instruction. See Col. 14, lines 58-65.

As per Claims 6 and 13, Goettelmann et al. disclose the step of translating without testing the memory address of the target instruction if the test can be safely eliminated. See Col. 13, 48-56.

As per Claims 7 and 14, Goettelmann et al. disclose the step of translating without testing a memory address of the target instruction if the memory address is on the same memory page. See Col. 13, 25-28.

As per Claim 15, Goettleman et al. disclose a computer that translates instructions from a target instruction set to a host instruction set, a method for determining validity of a translated instruction comprising:

Testing a memory address of a target instruction to be executed against a memory address associated with a translation of a target instruction, wherein said translation is linked to a translation of another target instruction (See Col. 4, lines 26-38 for the inter-procedural analysis or the linking of common procedures or instructions executed in the same sequence together, and generating a tree defining these procedural or linking relationships. See Col. 9, lines 43 et Seq. for the mapping action determining the validity of the memory addresses of the translated instructions).

Executing said translation if said memory addresses compare (See Col. 9, lines 54 et Seq. where the mapped instruction is executed in the address mapping refers to appropriated locations of the target machine's RAM);

And generating an exception if said memory addresses do not compare (See Col. 9, lines 54 et Seq. the system call if the instruction does not map and passing control to the system

simulation for determining the correct address by checking the target machine. An exception is a system call).

8. Claims 1-2, 5-9, and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by de Nicolas et al. U.S. Patent No. 5,167,023.

As per Claims 1 and 8, de Nicolas et al. recite translating an instruction set from a target computer to the host computer and validating the translation by testing the memory address and executing the translation or generating an exception based on the test. See Col. 5, lines 38-46 and Col. 12, lines 48-53.

As per Claims 2 and 9, de Nicolas et al. disclose the step of testing a memory address of the translated instruction in a process separate from translating the target instruction. See Col 5, lines 59-63 and Col. 6, lines 1-7

As per Claims 5 and 12, de Nicolas et al. disclose the step copying and storing the memory address of the target instruction. See Col. 13, lines 38-43.

As per Claims 6 and 13, de Nicolas et al. disclose the step of translating without testing the memory address of the target instruction if the test can be safely eliminated. See Col. 13, 45-50.

As per Claims 7 and 14, de Nicolas et al. disclose the step of translating without testing a memory address of the target instruction if the memory address is on the same memory page. See Col. 15, 20-31.

9. Claims 1-3, 5-10 and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Fogg, Jr. et al. U.S. Paten No. 4,951,195.

As per Claims 1 and 8, Fogg, Jr. et al. recite translating an instruction set from a target computer to the host computer and validating the translation by testing the memory address and executing the translation or generating an exception based on the test. See Col. 8, lines 65-69 and Col. 9, lines 15-23.

As per Claims 2 and 9, Fogg, Jr. et al. disclose the step of testing a memory address of the translated instruction in a process separate from translating the target instruction. See Col 11, lines 45-55.

As per Claims 3 and 10, Fogg, Jr. et al. disclose the step testing the memory address of a target instruction as part of the translation of the target instruction. See Col. 15, line 56- Col.16, line 34 and Figure 9.

As per Claims 5 and 12, Fogg, Jr. et al. disclose the step copying and storing the memory address of the target instruction. See Col. 10, lines 10-143.

As per Claims 6 and 13, Fogg, Jr. et al. disclose the step of translating without testing the memory address of the target instruction if the test can be safely eliminated. See Col. 17, 1-5.

As per Claims 7 and 14, Fogg, Jr. et al. disclose the step of translating without testing a memory address of the target instruction if the memory address is on the same memory page. See Col. 15, 56-61.

Conclusion

10. 10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samarina Makhdoom whose telephone number is 703-305-7209. The examiner can normally be reached on Full Time on Tuesday, Thursday, Friday, and Sunday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J. Teska can be reached on 703-305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0040 for regular communications and 703-305-0040 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

SM
December 8, 2002

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER